REMARKS

Reconsideration of pending Claims 101-116 and 123-223 is respectfully requested.

Claims 101, 103-107, 110-116, 123-126, 129, 131-135, 141-143, 149, 160, 163-164, 173, 176, 179, 182, 186, and 190 have been amended. New Claims 194-223 have been added. No new matter has been added with the amendments or the addition of the new claims.

Claims 117-122 have been cancelled without prejudice to their future prosecution. These claims are subject to restriction and within a non-elected group of claims (species Group "b" - Office Action mailed July 1, 2002). Applicant reserves the right to file a divisional on the non-elected claims.

The claims have been amended to replace the phrase "epitaxially grown silicon" with "epitaxial silicon" as supported in the original claims as filed (e.g., Claim 2: "epitaxial layer" and the specification, e.g., "...by growing one or more layers of epitaxial silicon" (at page 14, lines 24-25).

Support for the new Claims (including product-by-process Claims 203-223) is in the original claims and specification as follows:

Claim		**Support**
203-223	"...stacked"	page 7, line 3
213, 216-219, 221-223	"...depositing a conductivity enhancing dopant"	Claims 104, 111, 117, etc. page 4, lines 15-17; page 5, lines 13-15; pages 14-15, bridging sentence
204-212, 215-223	"...no subsequent removal..."	Claim 79
214, 220	"...doping...by ion implantation"	Claims 24, 77, etc. page 4, line 15 pages 14-15, bridging sentence
206-212, 215	"...preceding epitaxial layer"	page 14, line 21
208-210, 215	"...silicon precursor gas..."	page 9, line 20 to page 10, line 17 Claims 10-13
211, 212, 221, 222	"...rapid thermal oxidation" "...rapid thermal nitridation"	Claims 38-41, 68-69 pages 10-11, bridging paragraph

The amendments are intended to merely clarify language used in the claims, and the scope of the claims is intended to be the same after the amendment as it was before the amendment.

In the Office Action, page 4 paragraph 7, the Examiner stated:

> For the purpose of the examination, the examiner assumes that ~~each~~ epitaxial layer STACK comprises a top surface and sidewalls.

To clarify, as recited in the claims, each epitaxial layer comprises a top surface and sidewalls — the sidewalls having an insulative material disposed thereon. The Examiner is also directed to the specification, for example, at page 2, line 17 to page 3, line 9, for the description of an embodiment of a structure that is formed according to the invention, as well as the pictorial illustrations of the structures in the Figures.

Rejections under 35 U.S.C. § 112(1).

The Examiner rejected Claims 123-128, 143-148, 149-155, 167-168, 170-172, 176-178, 179-181, 186-189, and 190-193 under Section 112(1) for lack of enablement. This rejection is respectfully traversed.

The Examiner maintains that the claims are not enabled for "sidewalls with an overlying layer of an insulative material" on the basis that that phrase is not specifically stated in the specification.

The subject matter of the claim need not be described literally, i.e., using the same term (or *in haec verba*) as in the specification. The test for sufficiency of support of terms in the claims is whether the specification reasonably conveys to those skilled in the art, the invention as claimed. *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991). MPEP §§ 2163 and 2163.02.

The Examiner has the initial burden of presenting evidence or reasons — not just a bare assertion — why persons skilled in the art would not understand what is recited in the claims.

Claims 123, 143, 149, 176, 179, 186 and 190 have been amended to more clearly recite that the epitaxial layers have a top surface and sidewalls, and "*insulative material over the sidewalls*." That feature is supported in the specification at page 2, lines 11-12 ("The present method employs insulative spacers formed over the sidewalls of the epitaxial layers..."), and the Figures such as FIG. 1G, which illustrate insulative material (in the form of spacers) 44a, 44b, overlying the sidewalls 40a, 40b of the epitaxial layers 36a, 36b.

One skilled in the art, reading Applicant's written description and observing the pictorial representations in the drawings, would readily understand the meaning of the phrase "insulative material over the sidewalls" in the context of the claims and Applicant's description, and would be fully enabled to practice Applicant's invention as it is claimed. Applicant's claims are sufficiently supported by the specification. It is submitted that the pending claims are fully enabled, and withdrawal of this rejection is respectfully requested.

Rejections under 35 U.S.C. §112(2)

The Examiner rejected Claims 123-128, 143-148, 149-155, 167-168, 170-172, 176-178, 179-181, 186-189, and 190-193 under Section 112(2) for the use of indefinite claim language. This rejection is respectfully traversed.

The Examiner maintains that the phrase "sidewalls with an overlying layer of an insulative material" is unclear because such overlying layer of insulative material would prevent electrical conductivity.

The function of the insulative spacers on the sidewalls of the epitaxial layer is to eliminate lateral growth so that the epitaxial layer will grow vertically to form a pillar structure.

The Examiner is respectfully directed to the specification, for example, at page 2, lines 5-13 (emphasis added):

> The invention utilizes selective epitaxial growth (SEG) to form vertically oriented structures on semiconductor substrates. Crystal growth by SEG along a select facet to form a vertically oriented structure cannot be controlled by varying the growth conditions due to the existence of facets on the crystal having different orientations i.e., (100), (110), (111). However, such control is needed to achieve vertically oriented epitaxial growth *and eliminate lateral or horizontal growth that can short circuit closely positioned adjacent*

> *devices.* ***The present method employs insulative spacers formed over the sidewalls of the epitaxial layers to eliminate unwanted lateral growth and control the growth of the epitaxial film.***

This is further stated at page 4, lines 10-17:

> Additional epitaxial layers can be added by repeating the SEG step, and depositing the insulative layer, and selectively removing the insulative layer ***to maintain insulative material along the sidewalls as spacers to limit the growth of the epitaxial layer in a vertical orientation, resulting in a pillar-like gate structure having a desired height.*** A source region can then be formed by SEG above the uppermost epitaxial layer of the gate. To do so, a conductivity enhancing dopant can be added while the epitaxial layer is being deposited, or after the formed epitaxial layer is formed, for example, by ion implantation.

And also at page 11, lines 19-21:

> ...The spacer 44a previously formed along the sidewall 40a of the crystal 36a serves to prevent epitaxial growth of silicon crystals in a lateral or horizontal direction from the sidewall 40a.

Applicant is claiming structure composed of overlying layers of epitaxial silicon — each epi layer having a top surface and sidewalls with insulative material disposed on the sidewalls. It is pointed out that there is *no* insulative material disposed between overlying epitaxial layers.

The terms used in the claims are clear in their meaning and the language in the claims is definite and correct. Accordingly, it is submitted that the claims fully comply with the requirements of Section 112(2), and withdrawal of this rejection is respectfully requested.

Rejection of Claims under 35 U.S.C. 103(a)

The Examiner rejected Claims 101-109, 110-116, 123-128, 149-155 and 179 under Section 103(a) as obvious over JP 2001068671 (**Ri**) in view of US 5,902,125 (**Wu**). The Examiner rejected Claims 129-130, 132-135, 140-142, 143, [158-160, 165-166,] 173, [175], 182-185, 187-189, and 190-193 under Section 103(a) as obvious over **Ri** in view of US 5,970,351 (**Takeuchi**). The Examiner rejected Claim 131 under Section 103(a) as obvious over **Ri** in view of US 5,963,822 (**Saihara**). The Examiner rejected Claims 129, 137-139, 156-157, and 173-174 under Section 103(a) as obvious over **Wu**. These rejections are

respectfully traversed. Applicant's claims are directed to vertical structures (e.g., transistor, source/drain) that comprise two or more *overlying layers of epitaxial silicon*, each layer comprising a top surface and insulated sidewalls, with the uppermost epitaxial layer having top surface that is also insulated.

Epitaxial silicon. First of all, the Examiner maintains that the phrase "epitaxially grown silicon" in the claims is a process limitation that does not carry weight in the presently claimed structures. It is pointed out that the claims have been amended to recite the term "epitaxial silicon" in order to eliminate a purported process limitation from the claims.

Epitaxial silicon is not the same as other silicon forms and can be distinguished, for example, based on the structure and appearance of the layers, and by physical properties (e.g., electrical behavior). For example, an epitaxial silicon film has a single crystalline structure, and can be distinguished by the presence of a faceted top surface. The structure of an epitaxial film on a substrate can be examined by cross-sectioning and, for example, by scanning electron microscope (SEM) or transmission electron microscope (TEM), as known and used in the art. (This is discussed in the specification at page 9, lines 16-19.)

By comparison, neither polysilicon nor amorphous silicon have a single-crystal film structure and do not possess a crystal oriented facet on the top surface. The crystal orientation of a stack composed of epitaxial silicon is very different from that of either amorphous silicon or polycrystalline silicon. Thus, stacked epitaxial silicon layers can be readily distinguished from other stacked silicon films such as a stacked amorphous silicon (SAS) structure, or stacked polycrystalline silicon layers.

In addition, epitaxial silicon can be distinguished from other silicon forms by its properties. For example, Wu (cited by the Examiner) distinguishes epitaxial silicon from amorphous silicon based on dopant penetration into the respective materials. Wu teaches that amorphous silicon *suppresses penetration* of dopant (at col. 2, lines 4-20; emphasis added):

> Further, in order to achieve...Unfortunately, the effect of boron penetration through the thin gate oxide into Si substrate will degrade the device performance. *Prior art approaches to overcome these problems have resulted in the development of stacked-amorphous-silicon (SAS) film to suppress the boron penetration into ultra-thin gate oxide.* ...The SAS gate

> capacitor exhibits a smaller flat-band voltage shift, a less charge trapping and interface state generation rate than those of the as-deposited poly-Si gate capacitor. The main reason of the suppression of the boron or fluorine penetration by using SAS is because that the SAS structure exhibits the dopant segregation at the stacked-Si boundaries and a longer path for dopant diffusion to the interface between silicon and oxide.

Wu also discloses that the doping step results in implanting dopant into the SAS layer, *into the epitaxial silicon, and into the silicon substrate underlying the epitaxial silicon* (at col. 4, lines 55-59; emphasis added):.

> Referring to FIG. 5, the ARC layer 10 is then removed to expose the top of the SAS layer 8. Then, a blanket ion implantation is carried out to implant p-type dopant, such as boron or BF_2 into the SAS layer 8, the epitaxial silicon 16 *and silicon substrate 2 that under the epitaxial silicon 16*...

As Wu describes, epitaxial silicon *allows penetration* of dopant into the underlying substrate. By comparison, the properties of amorphous silicon *inhibit* dopant penetration into the underlying substrate. Thus, the character and properties of epitaxial silicon are *necessarily different* than the character and properties of amorphous silicon, as Wu has described.

In addition, doped polysilicon film resistivities are less than those of equally doped epitaxial silicon

Epitaxial silicon is *not* the same as amorphous silicon or polycrystalline silicon based on either appearance and/or properties.

Ri combined with Wu. With regard to the rejection of Claims 101-109, 116 and 180 (*transistor gate* of overlying epi layers) based on Ri combined with Wu, the Examiner admits that Ri does *not* disclose a structure comprising at least two overlying layers of epitaxial silicon and an uppermost layer having an insulated top surface.

However, the Examiner asserts that Wu discloses *a transistor 8 comprising at least two overlying layers of silicon* (citing to col. 4, line 3), and an uppermost layer having an insulated top surface (citing to FIG. 8). The Examiner maintains that is would have been obvious to combine "Wu's teaching of multiple silicon layers with Ri's device because it

would have prevented the penetration of the dopant through, as taught by Wu" (col. 4, line 17-18).

Both Ri and Wu disclose a gate with an adjacent elevated source and drain composed of an epitaxial silicon layer. Wu teaches an *etched* gate structure composed of stacked *amorphous silicon* (SAS) layers 8. (See FIG. 2, and below at FIG. 5)[1]

There is no motivation in either Ri or Wu to substitute epitaxial silicon for amorphous silicon to form the stacked gate structure described by Wu. Wu essentially *teaches away* from using epitaxial silicon to form the gate structure. Wu specifically teaches the importance of forming the gate with amorphous silicon based on the ability of amorphous silicon to *suppress* boron penetration through a gate oxide layer and into the underlying silicon substrate to overcome problems in the prior art (Wu at cols. 1-2, bridging paragraph; emphasis added):

> Further, in order to achieve ... Unfortunately, the effect of boron penetration through the thin gate oxide into Si substrate will degrade the device performance. Prior art approaches to overcome these problems have resulted in the development of stacked-amorphous-silicon (SAS) film to suppress the boron penetration into ultra-thin gate oxide. As seen in "Suppression of Boron Penetration into an Ultra-Thin Gate Oxide by Using a Stacked-Amorphous-Silicon (SAS) Film, Shye Lin Wu, 1993, IEDM, p. 329". In this paper, Wu suggests that the use of stacked-amorphous-silicon (SAS) can suppress the boron penetration through an ultra-thin oxide. The *SAS* gate capacitor exhibits a smaller flat-band voltage shift, a less charge trapping and interface state generation rate than those of the as-deposited *poly-Si* gate capacitor. The main reason of the suppression of the boron or fluorine penetration by using SAS is because that the SAS structure exhibits the dopant segregation at the stacked-Si boundaries and a longer path for dopant diffusion to the interface between silicon and oxide.

Based on the information in Wu, there is no motivation to alter either Wu or Ri form a gate structure composed of overlying epitaxial layers, as in Claims 101-109 and 116 (or 180).

[1] As Wu illustrates in FIG. 1, the amorphous silicon (SAS) layer 8 is formed by a blanket deposition process on a substrate, and covered by an ARC layer 10. The SAS layer 8 is then etched to form the gate structure.

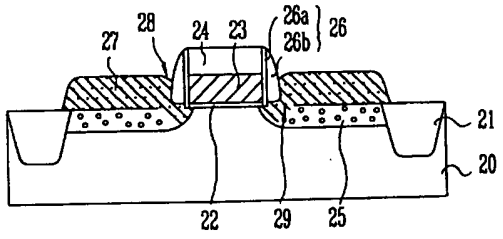
Furthermore, the Examiner's proposed combination of Wu's multiple silicon layers with Ri's device because "it would have prevented the penetration of the dopant through" (Office Action at page 5, last paragraph) would not provide an elevated gate composed of overlying epitaxial silicon layers, as in Claims 101-109 and 116 (or 180). Wu specifically teaches the use of *stacked amorphous silicon* (SAS) layers to form a gate structure. The substitution of Wu's gate structure into Ri's device would result in a stacked SAS gate — not a stacked epitaxial silicon gate as claimed by Applicant.

Accordingly, withdrawal of the rejection of Claims 101-109 and 116 based on Ri combined with Wu is respectfully requested.

As for Claims 110-116 and 123-128 (*source/drain* of overlying epi layers), there is nothing in the teachings of either Ri or Wu that would motivate one to form an S/D structure of overlying epitaxial silicon layers.

As admitted by the Examiner — Ri does *not* disclose a structure comprising at least two overlying layers of epitaxial silicon. Ri describes a gate structure with an adjacent elevated drain composed of a *single* epitaxial silicon layer 27. This is illustrated by FIG. 3C, shown below:

FIG. 3C



Similarly, Wu — like Ri — describes a gate structure with an adjacent elevated source and drain made of a ***single*** epitaxial silicon layer 16 (and an extended source and drain 22 — formed by doping — in the substrate) (Wu at col. 4, line 48 to col. 5, line 14). The source/drain structure 18, 22 of Wu is illustrated in FIGS. 5-6, shown below:

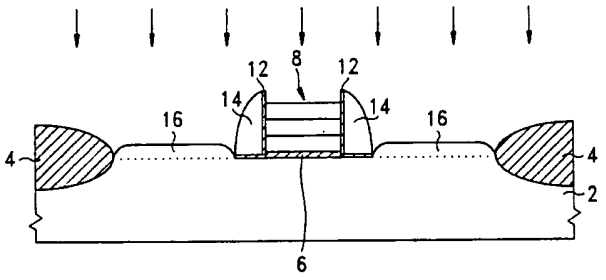


FIG.5

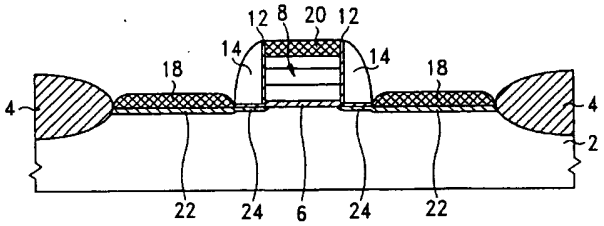


FIG.6

Neither Ri nor Wu teach or suggest a source/drain comprising two or more layers of epitaxial silicon. Both teach a ***single*** layer of epitaxial silicon to form the source/drain.

Furthermore, neither Ri nor Wu teach *insulative spacers* on the sidewalls of the epitaxial layer of the S/D structure. The Examiner cites to FIG. 8 of Wu as disclosing "an uppermost layer having an insulated top surface." (This is also illustrated in FIG. 7 below.)

Wu describes forming a thick oxide layer 26 over the substrates and gate structure for isolation (col. 5, lines 15-19):

> Referring to FIG. 7, a thick oxide layer 26 is formed over the substrate 2 and gate structure for isolation. For example, CVD oxide can be used for in this step. Then, contact

holes 28 are generated in the oxide layer 26 and aligned to the source and drain 22 by using conventional manner.

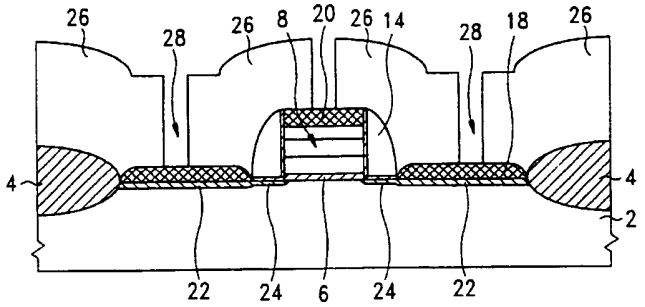


FIG.7

Although Wu teaches an oxide layer 26 formed over the source and drain 18 — the oxide layer is disposed over a *single* epitaxial layer.

The present invention utilizes insulative spacers on the sidewalls of each epitaxial layer and no insulative layer between overlying epitaxial layers, which achieves Applicant's structures as claimed. As disclosed by Applicant (see specification at page 2, lines 5-13; emphasis added):

> The invention utilizes selective epitaxial growth (SEG) to form vertically oriented structures on semiconductor substrates. Crystal growth by SEG along a select facet to form a vertically oriented structure cannot be controlled by varying the growth conditions due to the existence of facets on the crystal having different orientations i.e., (100), (110), (111). However, such control is needed to achieve vertically oriented epitaxial growth and eliminate lateral or horizontal growth that can short circuit closely positioned adjacent devices. The present method employs *insulative spacers* formed over the sidewalls of the epitaxial layers *to eliminate unwanted lateral growth* and control the growth of the epitaxial film.

The sidewall spacers limit the position of a successive epitaxial layer to the exposed top surface of the underlying (previous) epitaxial layer. Due to the presence of the insulative spacers on the sidewalls of each underlying epitaxial layer, *lateral or horizontal crystals* are eliminated. Thus, the resulting structure is composed of overlying epitaxial layers in a vertical orientation.

Wu's disclosure of forming an oxide layer 26 over the epitaxial layer 18 would *not* result in Applicant's source/drain structure comprising overlying multiple layers of epitaxial silicon extending in a vertical plane from the surface, as recited in Claims 110-116 and 123-128. Nor would it result in a "*structure*" comprising overlying epitaxial silicon layers, as recited in Claims 149-155 and 179.

Finally, the Examiner's proposed combination of Wu's teaching of multiple silicon layers with Ri's device because "it would have prevented the penetration of the dopant through" (Office Action at page 5, last paragraph) is *clearly without basis* with regard to Claims 110-116 and 123-128 directed to an elevated S/D of overlying epi layers.

Wu teaches a source/drain composed of a single epitaxial silicon layer 16, and then doping the epitaxial layer 16 *and the underlying substrate 2* to form the source/drain 22 and an extended source and drain junction 24 (see above at FIG. 6).

Ri teaches forming a doped region 25 in the substrate and doped regions 27a, 27b within the epitaxial layer 27 (see above at FIG. 3C, and below at FIG. 3D).

Neither Ri nor Wu teach preventing dopant penetration into the substrate with respect to a source/drain structure. Clearly, the Examiner's position is without any basis.

In sum, the combination of Ri with Wu does not teach or suggest Applicant's structures as recited in the claims, and withdrawal of this rejection is respectfully requested.

Ri combined with Takeuchi. Next, the Examiner rejected Claims 129-130, 132-135, 140-142, 143, 173, 182-185, 187-189, and 190-193 (a *structure* comprising overlying epitaxial silicon layers) as obvious over Ri combined with Takeuchi.

The Examiner erroneously states that Ri discloses a structure in FIG. 3D that comprises "at least two overlying layers 27a and 27b of epitaxial grow [sic] silicon, each epitaxial layer having insulated sidewalls 26."

First of all, the Examiner expressly *admitted* that Ri does not disclose overlying epitaxial layers — in the Office Action at page 5 (par. 8) (emphasis added):

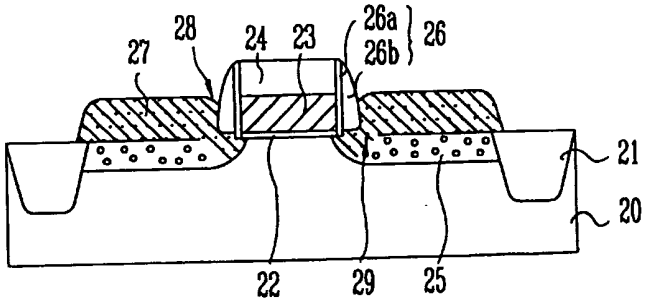
> But Ri references *does not expressly disclose* a transistor gate 23 comprises [sic] at least two overlying layers of epitaxial silicon and an uppermost layer having an insulated top surface.

Secondly, as discussed above, Ri describes a transistor comprising a gate structure and an elevated drain comprising a *single* epitaxial silicon layer 27.

Referring to FIG. 3C (shown below), Ri forms a *single* epitaxial silicon layer 27, which is lightly doped (page 14, lines 3-13; emphasis added):

> After the hydrogen bake, the lightly doped silicon layer or lightly doped epitaxial silicon layer 27 is formed overlying the mediumly doped regions 25. In one embodiment, the lightly doped silicon layer 27 is formed by selectively growing an epitaxial layer on the exposed portion of the silicon substrate 20 using a low pressure chemical vapor deposition ("LPCVD") method. ... The deposition process is performed for about 10 minutes to provide *the lightly doped epitaxial silicon layer 27* having a thickness between about 500 Å and 2000 Å.

FIG. 3C



Referring to FIG. 3D, an *ion implantation step* is then performed to form heavily doped *region* 27a within the epitaxial layer 27.[2] The ion implantation step includes injecting

[2] Ri also states that the doped regions 27a, 27b can be formed without an ion implantation step — by CVD process involving light doping and then heavy doping. That process still forms two *regions* — not separate epitaxial layers (Ri at page 15, lines 14-17; emphasis added):

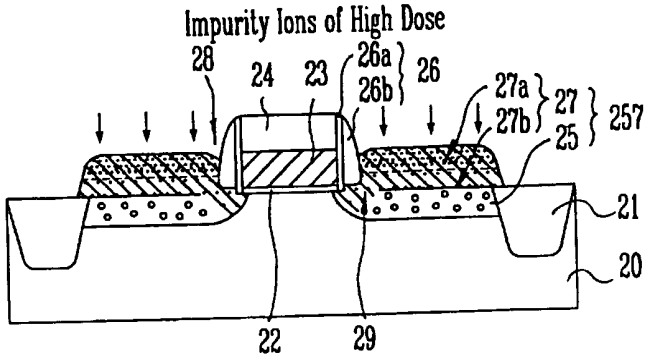
> In one embodiment, the heavily doped *regions 27a* and the lightly doped *regions 27b* may be formed without ion implantation step. For example, *these regions may be formed* by performing a first CVD method to grow the lightly doped region 27b and then switching to a second CVD method to grow the heavily doped regions 27a.

Ri does not disclose forming two separate epitaxial layers.

arsenic ions into the epitaxial silicon layer. See Ri at page 15, lines 2-8 and 18-20 (emphasis added):

> Referring now to FIG. 3D, an ion implantation step is performed to form heavily doped *regions 27a* on the epitaxial silicon layer 27. In one embodiment, to manufacture NMOS transistors, the ion implantation step includes injecting arsenic ions into the epitaxial silicon layer at low energy of about 5 KeV to about 10 KeV, i.e., into the depth of about 300 Å. The energy level is selected so that the ions are not driven too far into the epitaxial silicon layer, so that the lower portion of the epitaxial silicon layer remains lightly doped...
>
> ...
>
> Referring back to the above embodiment, the annealing process is controlled so that the upper portion of the epitaxial silicon layer 27 becomes heavily doped while the lower portion remains lightly doped...

FIG. 3D



Thus, the *single* epitaxial silicon layer 27 includes two doped *regions* — a heavily doped *region 27a*; and a lightly doped *region 27b*— not separate and overlying epitaxial layers.

Contrary to the Examiner's assertion, Ri does *not* describe two overlying layers of epitaxial silicon. Rather, Ri describes a *single layer* of epitaxial silicon comprising two dopant regions within the single layer.

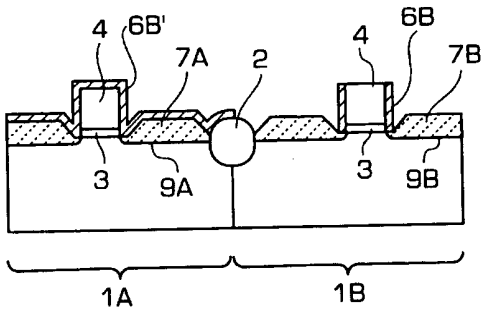
Nor does Ri teach *insulative spacers* on the sidewalls of the epitaxial layer of the S/D structure. As shown in FIG. 3D (above), there are no sidewall spacers on the epitaxial layer 27 of Ri.

Similarly, Takeuchi — like Ri — describes a gate with adjacent elevated source and drain 7A made of a "silicon single crystal thin film" which is then covered with an insulator 6B' (see at col. 11, line 48 to col. 12, line 2; emphasis added):

> According to the method of production...In the method of production, ***a silicon single crystal thin film*** doped with arsenic or phosphor ***is selectively grown*** in an area which is for making the source and drain region of the n-channel transistor ***to form n-type elevated source and drain 7A***. By this process, facet 8A is formed on elevated source and drain 7A (FIG. 11(a)). ...Then, as shown in FIG. 11(b), second insulators 6B' and 6B, which cover the entire n-channel transistor 1A and a side face of the gate of the p-channel transistor, are formed, ***and a silicon single crystal thin film*** doped with boron is selectively grown only in a region which is for making the source and drain region of the p-channel transistor ***to form p-type elevated source and drain 7B***. By this process, facet 8B is formed (FIG. 11(b)). ...

Takeuchi's elevated source/drain 7A, 7B are illustrated in FIG. 11(c), shown below:

FIG. 11(c)



It is also pointed out that elevated source and drain 7B is <u>not</u> covered with an insulated film.

Thus, although Takeuchi teaches an oxide layer 6B' formed over the source and drain 7A — the oxide layer is disposed over a *single* epitaxial layer.

As discussed above (with respect to Wu), Applicant's claimed structure has insulative spacers on the sidewalls of <u>each</u> of the overlying epitaxial layers. The sidewall spacers on an underlying epitaxial layer limit the successive epitaxial layer to a vertical orientation on the exposed top surface of the underlying epitaxial layer — and eliminate the presence of lateral or horizontally oriented crystals from the second (overlying) layer.

The teaching in Ri — of a source/drain composed of a single epitaxial layer, combined with Takeuchi's disclosure — of forming an oxide layer 6B' over a single epitaxial layer 7A, does not provide the requisite teaching of a structure composed of *at least two* overlying layers of epitaxial silicon with an insulative layer over the sidewalls of each of the epitaxial layers and no insulative layer between overlying epitaxial layers — with the structure extending in a vertical plane from the surface.

The combination of Ri with Takeuchi does not teach or suggest Applicant's claimed structure. Accordingly, withdrawal of this rejection is respectfully requested.

Ri combined with Saihara. Next, the Examiner rejected Claim 131 as obvious over Ri in combination with Saihara. Claim 131 depends from Claim 129 directed to a structure with overlying layers of epitaxial silicon, with the additional limitation that the facet has a (100) plane orientation.

The Examiner cites Saihara for disclosing that a silicon substrate has a plane orientation of (100) or (111). The Examiner maintains that it would be obvious to form the epitaxial layer 27a of Ri having a plane orientation of (100).

Saihara describes methods for forming a single epitaxial film layer on a surface of a (100) silicon substrate.

As the primary reference of Ri is inapplicable for the above-stated reasons (e.g., failing to teach at least two overlying epitaxial layers), combining the teaching of Saihara does not make up for the insufficiencies of Ri. Accordingly, withdrawal of this rejection is respectfully requested.

Wu (alone). Finally, the Examiner rejected Claims 129, 137-139, 156-157, and 173-174 as obvious over Wu.

First of all, in response to the Examiner's re-statement that process limitations "epitaxially grown silicon" in Claim 129 does not carry weight in a claim drawn to a structure — it is again pointed out that the claims have been amended to recite the term "epitaxial

silicon" in order to eliminate a purported process limitation from the claims. The Examiner is also directed to the previously stated remarks addressing epitaxial silicon.

As for the rejection of the claims, the Examiner cites to the gate in FIG. 8 of Wu, which is composed of overlying layers of silicon. The Examiner maintains that it would be obvious to *replace* the stacked-amorphous silicon (SAS) layer 8 with epitaxial silicon "because such epitaxial grown silicon would have been considered a mere substitution of art-recognized equivalent values." (emphasis added)

As discussed previously, Wu *teaches away* from using a silicon material other than amorphous silicon to form a gate structure.

To overcome problems in the prior art concerning boron penetration through a gate oxide layer and into the underlying silicon substrate — Wu specifically teaches the importance of forming the gate with amorphous silicon (Wu at cols. 1-2, bridging paragraph):

> Further, in order to achieve ... Unfortunately, the effect of boron penetration through the thin gate oxide into Si substrate will degrade the device performance. Prior art approaches to overcome these problems have resulted in the development of stacked-amorphous-silicon (SAS) film to suppress the boron penetration into ultra-thin gate oxide. As seen in "Suppression of Boron Penetration into an Ultra-Thin Gate Oxide by Using a Stacked-Amorphous-Silicon (SAS) Film, Shye Lin Wu, 1993, IEDM, p. 329". In this paper, Wu suggests that the use of stacked-amorphous-silicon (SAS) can suppress the boron penetration through an ultra-thin oxide. The SAS gate capacitor exhibits a smaller flat-band voltage shift, a less charge trapping and interface state generation rate than those of the as-deposited poly-Si gate capacitor. The main reason of the suppression of the boron or fluorine penetration by using SAS is because that the SAS structure exhibits the dopant segregation at the stacked-Si boundaries and a longer path for dopant diffusion to the interface between silicon and oxide.

In addition, Wu explicitly teaches the benefits over the prior art by using a stacked amorphous silicon (SAS) structure as the gate (at col. 5, lines 27-35; emphasis added):

> *The present invention can provide various benefits over the prior art.* For example, the operation speed will be increased by the SALICIDE technology. The short channel effect will be suppressed by using the elevated source and drain junction, and the extended ultra-shallow source and drain junction. *Further, The p+ poly-Si gate with minimum boron penetration into thin gate oxide could be* ***achieved by using the stacked-amorphous-silicon structure as the poly gate.***

Clearly, based on the specific teachings stated by Wu — there is no motivation to substitute a different silicon material for amorphous silicon to form the gate structure of Wu's transistor device. In particular, there would no motivation to substitute epitaxial silicon for amorphous silicon in the gate structure taught by Wu.

The purpose of the amorphous silicon in the gate structure of Wu is to *prevent* dopant diffusion into the underlying substrate. Wu further discloses that the doping step resulted in implanting dopant into the SAS layer, *into the epitaxial silicon, and into the silicon substrate underlying the epitaxial silicon*. Again, as stated in Wu at col. 4, lines 55-59 (emphasis added):

> Referring to FIG. 5, the ARC layer 10 is then removed to expose the top of the SAS layer 8. Then, a blanket ion implantation is carried out to implant p-type dopant, such as boron or BF_2 ***into the SAS layer 8, the epitaxial silicon 16 and silicon substrate 2 that under the epitaxial silicon 16...***

As Wu discloses, in contrast to amorphous silicon, which *inhibits* dopant penetration into the underlying substrate — epitaxial silicon *allows penetration* of dopant into the underlying substrate.

Clearly, one reading the disclosure in Wu would *not* be motivated to substitute epitaxial silicon for the amorphous silicon in Wu's gate structure.

Based on those teachings in Wu, the Examiner's proposed substitution of epitaxial silicon for Wu's multiple amorphous silicon layers is clearly without basis. Accordingly, withdrawal of the rejection of Claims 129, 137-139, 156-157, and 173-174 based on Wu is respectfully requested.

None of the cited references, either alone or in combination, teach or suggest Applicant's raised structures as claimed. Accordingly, withdrawal of these rejections is respectfully requested.

Extension of Term.

The proceedings herein are for a patent application and the provisions of 37 CFR § 1.136 apply. Applicant believes that no extension of term is required. However, this

conditional petition is being made to provide for the possibility that Applicant has inadvertently overlooked the need for a petition for extension of time. If any extension and/or fee are required, please charge Account No. 23-2053.

Applicant believes that the claims are in condition for allowance, and notification to that effect is respectfully requested.

Respectfully submitted,

Kristine Strodthoff

Kristine M. Strodthoff
Registration No. 34,259

Dated: February 20, 2003

P.O. ADDRESS:

WHYTE HIRSCHBOECK DUDEK S.C.
111 East Wisconsin Avenue, Suite 2100
Milwaukee, Wisconsin 53202
(414) 273-2100

Customer No. 022202

OIPE JC23 FEB 2 0 2003 PATENT & TRADEMARK OFFICE

Blacklined Claims

OIPE JC23 FEB 2 0 2003 PATENT & TRADEMARK OFFICE

WHAT IS CLAIMED IS:

101. (amended) A transistor in a semiconductor device, comprising:

source/drain diffusion regions formed on a semiconductive region of a substrate; and

a transistor gate formed on the semiconductive region between the source/drain diffusion regions, the transistor gate extending in a vertical orientation from the substrate, the transistor gate comprising at least two overlying layers of ~~epitaxially grown~~ epitaxial silicon, ~~each~~ including an uppermost epitaxial layer ~~having~~:

each epitaxial silicon layer comprising a top surface and insulated sidewalls, and ~~an~~ the uppermost epitaxial silicon layer having an insulated top surface.

102. The transistor of Claim 101, wherein the source/drain diffusion regions are elevated and extend in a vertical orientation from the substrate surface adjacent to the transistor gate.

103. (amended) The transistor of Claim 102, wherein each of the source/drain diffusion regions comprise at least two overlying layers of ~~epitaxially grown~~ epitaxial silicon, each epitaxial silicon layer having a top surface, and insulated sidewalls, and an uppermost epitaxial silicon layer having an insulated top surface.

104. (amended) The transistor of Claim 103, wherein the uppermost epitaxial silicon layer of the source/drain diffusion regions comprise ~~an uppermost epitaxial layer comprising~~ a conductivity enhancing dopant.

105. (amended) The transistor of Claim 103, wherein each of the epitaxial silicon layers of the source/drain diffusion regions comprise a conductivity enhancing dopant.

106. (amended) The transistor of Claim 101, wherein each epitaxial silicon layer comprises a faceted top surface.

107. (amended) The transistor of Claim 101, wherein each epitaxial silicon layer has a thickness of about 50 to about 200 nm.

108. The transistor of Claim 101, wherein the transistor is isolated within the substrate by at least one dielectric isolation region formed in the substrate adjacent thereto.

109. The method of Claim 108, wherein the at least one dielectric isolation region is a shallow trench isolation region comprising an oxide.

110. (amended) A transistor in a semiconductor device, comprising:

a transistor gate ~~formed~~ disposed on a semiconductive region of a substrate; and

elevated source/drain diffusion regions ~~formed~~ disposed on the semiconductive region adjacent to the transistor gate, and extending in a vertical plane from the substrate;

each of the source/drain diffusion regions ~~covered by a layer of insulative material and~~ comprising at least two overlying layers of ~~epitaxially grown silicon.~~ epitaxial silicon, including an uppermost epitaxial silicon layer; each epitaxial silicon layer comprising a top surface and insulated sidewalls, and the uppermost epitaxial silicon layer having an insulated top surface.

111. (amended) The transistor of Claim 110, wherein the source/drain diffusion regions comprise an uppermost epitaxial silicon layer comprising a conductivity enhancing dopant.

112. (amended) The transistor of Claim 110, wherein at least one of the epitaxial silicon layers of the source/drain diffusion regions comprise a conductivity enhancing dopant.

113. (amended) The transistor of Claim 112, wherein at least one of the epitaxial silicon layers comprises a concentration gradient of the dopant.

114. (amended) The transistor of Claim 110, wherein the epitaxial silicon layers comprise a faceted top surface.

115. (amended) The transistor of Claim 110, wherein each epitaxial silicon layer has a thickness of about 50 to about 200 nm.

116. (amended) The transistor of Claim 110, wherein the transistor gate is covered by a layer of insulative material and comprises at least two overlying layers of ~~epitaxially grown silicon.~~ epitaxial silicon.

~~117. A transistor in a semiconductor device, comprising:~~
~~a substrate having a buried drain region;~~
~~a gate overlying the buried drain region, the gate comprising multiple, vertically-oriented and overlying epitaxial layers and a top surface, each epitaxial layer having insulated sidewalls;~~
~~a source region overlying the top surface of the gate, the source region comprising an epitaxial layer doped with a conductivity enhancing dopant, and covered by a layer of insulative material.~~

~~118. The transistor of Claim 117, wherein each of the epitaxial layers of the gate is about 50 to about 200 nm thick.~~

~~119. The transistor of Claim 117, wherein the epitaxial layer of the source region is at least about 10 nm thick.~~

~~120. The transistor of Claim 117, wherein the epitaxial layers have a faceted top surface.~~

~~121. The transistor of Claim 117, wherein the buried drain comprises an n-type conductivity enhancing dopant an n-type selected from the group consisting of phosphine, arsine, and combinations thereof.~~

~~122. The transistor of Claim 117, wherein the buried drain region is about 50 nm to about 100 nm wide.~~

123. (amended) A transistor in a semiconductor device, comprising:

a transistor gate disposed on a semiconductive region of a substrate; and

an elevated source/drain diffusion region disposed on the substrate adjacent to the transistor gate in a vertical orientation from the substrate; the source/drain diffusion region comprising at least two overlying layers of ~~epitaxially grown silicon; each epitaxial layer having~~ epitaxial silicon, including an uppermost epitaxial layer; each of the at least two epitaxial silicon layers comprising a top surface~~,~~ and sidewalls~~,~~ with ~~an overlying~~ a layer of an insulative material~~,~~ disposed over the sidewalls; and the uppermost epitaxial layer having a top surface with an overlying layer of an insulative material.

124. (amended) The transistor of Claim 123, wherein at least one of the epitaxial silicon layers of the source/drain diffusion region comprises a conductivity enhancing dopant.

125. (amended) The transistor of Claim 124, wherein the uppermost epitaxial silicon layer of the source/drain diffusion region comprises a conductivity enhancing dopant.

126. (amended) The transistor of Claim 124, wherein at least one of the epitaxial silicon layers comprises a concentration gradient of the dopant.

127. The transistor of Claim 124, wherein the conductivity enhancing dopant comprises a p-type dopant.

128. The transistor of Claim 124, wherein the conductivity enhancing dopant comprises an n-type dopant.

129. ~~(~~(twice amended) A semiconductor structure, comprising:

at least two overlying layers of ~~epitaxially grown~~ epitaxial silicon, ~~each~~ including an uppermost epitaxial layer ~~having;~~ each epitaxial silicon layer comprising a top surface and insulated sidewalls, and ~~an~~ the uppermost epitaxial layer having an insulated top surface; the structure disposed on a substrate in a vertical orientation.

130. (amended) The semiconductor structure of Claim 129, wherein each epitaxial silicon layer comprises a top surface defining a facet.

131. (amended) The semiconductor structure of Claim ~~130~~ 129, wherein the facet has a (100) plane orientation.

132. (amended) The semiconductor structure of Claim 129, wherein each epitaxial silicon layer has a thickness of up to about 200 nm.

133. (amended) The semiconductor structure of Claim 132, wherein each epitaxial silicon layer has a thickness of about 50 to about 200 nm.

134. (amended) The semiconductor structure of Claim 132, wherein one or more epitaxial silicon layers has a thickness of about 70 to about 100 nm.

135. (amended) The semiconductor structure of Claim 132, wherein each epitaxial silicon layer has a thickness of at least about 10 nm to about 30 nm.

136. The semiconductor structure of Claim 129, being disposed adjacent to a gate or word line.

137. The semiconductor structure of Claim 129, being disposed adjacent to a source/drain region.

138. The semiconductor structure of Claim 137, being a transistor gate.

139. The semiconductor structure of Claim 138, wherein the transistor gate is isolated within the substrate by at least one dielectric isolation region disposed in the substrate adjacent thereto.

140. The semiconductor structure of Claim 129, being a source/drain diffusion region.

141. (amended) The semiconductor structure of Claim 140, wherein the uppermost epitaxial silicon layer comprises a conductivity enhancing dopant.

142. (amended) The semiconductor structure of Claim 140, wherein each of the epitaxial silicon layers comprises a conductivity enhancing dopant.

143. (amended) A semiconductor structure, comprising;

at least two overlying layers of ~~epitaxially grown~~ epitaxial silicon, each epitaxial silicon layer ~~having~~ comprising a top surface~~,~~ and sidewalls ~~with an overlying layer of an~~, and insulative material~~,~~ over the sidewalls; an uppermost epitaxial ~~layer~~ silicon layer of the at least two overlying layers having a top surface with an overlying layer of an insulative material; ~~and~~ wherein the structure is disposed on a substrate in a vertical orientation.

144. The semiconductor structure of Claim 143, wherein the insulative layer comprises an oxide film, a nitride film, an oxidized nitride film, or a composite oxide/nitride film.

145. The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon nitride film.

146. The semiconductor structure of Claim 145, wherein the silicon nitride film has a thickness of about 5 to about 20 nm.

147. The semiconductor structure of Claim 144, wherein the insulative layer comprises a silicon oxide film.

148. The semiconductor structure of Claim 147, wherein the silicon oxide film has a thickness of about 2 to about 5 nm.

149. (amended) A semiconductor structure, comprising:

at least two overlying layers of ~~epitaxially grown~~ epitaxial silicon, each epitaxial silicon layer ~~having~~ comprising a top surface, ~~and~~ sidewalls ~~with an overlying layer of~~, and an insulative material over the sidewalls; an uppermost epitaxial layer of the at least two overlying layers having a top surface with an overlying layer of an insulative material; one or more of the epitaxial silicon layers comprising a conductivity enhancing dopant; ~~and~~ wherein the structure is disposed on a substrate in a vertical orientation.

150. The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises a p-type dopant.

151. ~~(amended)~~ The semiconductor structure of Claim 150, wherein the p-type dopant is selected from the group consisting of diborane, boron trichloride, and boron trifluoride, and combinations thereof.

152. ~~(amended)~~ The semiconductor structure of Claim 149, wherein the conductivity enhancing dopant comprises an n-type dopant.

153. ~~(amended)~~ The semiconductor structure of Claim 152, wherein the n-type dopant is selected from the group consisting of phosphine, arsine, and combinations thereof.

154. ~~(amended)~~ The semiconductor structure of Claim 149, wherein one or more of the epitaxial layers comprises a concentration gradient of the dopant within the epitaxial layer.

155. ~~(amended)~~ The semiconductor structure of Claim 154, wherein the concentration gradient comprises a low to high concentration of the dopant within the epitaxial layer, with the high dopant concentration at the top surface of the layer.

156. ~~(new)~~ The semiconductor structure of Claim 129, being a component of a transistor.

157. ~~(new)~~ The semiconductor structure of Claim 156, being a transistor gate.

158. ~~(new)~~ The semiconductor structure of Claim 156, being a source/drain diffusion region.

159. ~~(new)~~ The semiconductor structure of Claim 158, wherein at least one of the epitaxial layers of the source/drain diffusion regions comprises a conductivity enhancing dopant.

160. ~~(new)~~(amended) The semiconductor structure of Claim 159, wherein at least one of the epitaxial silicon layers of the source/drain diffusion regions comprises a concentration gradient of a conductivity enhancing dopant.

161. ~~(new)~~ The semiconductor structure of Claim 157, wherein the transistor gate is disposed over a drain region disposed in the substrate.

162. ~~(new)~~ The semiconductor structure of Claim 161, the drain region is about 50 nm to about 100 nm wide.

163. ~~(new)~~(amended) The semiconductor structure of Claim 161, wherein the uppermost epitaxial silicon layer of the transistor gate structure comprises a source region doped with a conductivity enhancing dopant.

164. ~~(new)~~(amended) The semiconductor structure of Claim 163, wherein the uppermost epitaxial silicon layer is at least about 10 nm thick.

165. ~~(new)~~ The semiconductor structure of Claim 156, wherein the transistor is isolated within the substrate by at least one dielectric isolation region formed in the substrate adjacent thereto.

166. ~~(new)~~ The semiconductor structure of Claim 165, wherein the at least one dielectric isolation region is a shallow trench isolation region comprising an oxide.

167. ~~(new)~~ The semiconductor structure of Claim 143, being a component of a transistor.

168. ~~(new)~~ The semiconductor structure of Claim 167, being a transistor gate.

169. ~~(new)~~ The semiconductor structure of Claim 167, being a source/drain diffusion region.

170. ~~(new)~~ The semiconductor structure of Claim 149, being a component of a transistor.

171. ~~(new)~~ The semiconductor structure of Claim 170, being a transistor gate.

172. ~~(new)~~ The semiconductor structure of Claim 170, being a source/drain diffusion region.

173. ~~(new)~~(amended) A semiconductor structure, comprising:

at least two overlying layers of ~~epitaxially grown silicon, each epitaxial layer having insulated sidewalls, and~~ epitaxial silicon including an uppermost epitaxial silicon layer; each

epitaxial silicon layer comprising a top surface and insulated sidewalls, and the uppermost epitaxial silicon layer having an insulated top surface; the structure disposed on a substrate in a vertical orientation; the structure being a component of a transistor.

174. ~~(new)~~ The semiconductor structure of Claim 173, being a transistor gate.

175. ~~(new)~~ The semiconductor structure of Claim 173, being a source/drain diffusion region.

176. ~~(new)~~(amended) A semiconductor structure, comprising:

at least two overlying layers of ~~epitaxially grown~~ epitaxial silicon, each epitaxial silicon layer ~~having~~ comprising a top surface, ~~and~~ sidewalls ~~with an overlying layer of an~~, and insulative material~~,~~ over the sidewalls; an uppermost epitaxial ~~layer~~ silicon layer of the at least two overlying layers having a top surface with an overlying layer of an insulative material; the structure disposed on a substrate in a vertical orientation; the structure being a component of a transistor.

177. ~~(new)~~ The semiconductor structure of Claim 176, being a transistor gate.

178. ~~(new)~~ The semiconductor structure of Claim 176, being a source/drain diffusion region.

179. ~~(new)~~(amended) A semiconductor structure, comprising:

at least two overlying layers of ~~epitaxially grown~~ epitaxial silicon, each epitaxial silicon layer ~~having~~ comprising a top surface, ~~and~~ sidewalls ~~with an overlying layer of an~~, and insulative material over the sidewalls; an uppermost epitaxial ~~layer~~ silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; one or more of the at least two epitaxial silicon layers comprising a conductivity enhancing dopant; the structure disposed on a substrate in a vertical orientation; and the structure being a component of a transistor.

180. ~~(new)~~ The semiconductor structure of Claim 179, being a transistor gate.

181. ~~(new)~~ The semiconductor structure of Claim 179, being a source/drain diffusion region.

182. ~~(new)~~(amended) A semiconductor device, comprising:

a structure comprising at least two overlying layers of ~~epitaxially grown~~ epitaxial silicon, each epitaxial ~~layer having~~ silicon layer comprising a top surface and insulated sidewalls, and an uppermost epitaxial ~~layer~~ silicon layer of the at least two overlying epitaxial silicon layers having an insulated top surface; the structure disposed on a substrate in a vertical orientation.

183. ~~(new)~~ The semiconductor device of Claim 182, comprising a transistor.

184. ~~(new)~~ The semiconductor device of Claim 183, wherein the structure comprises a transistor gate.

185. ~~(new)~~ The semiconductor device of Claim 183, wherein the structure comprises a source/drain diffusion region.

186. ~~(new)~~(amended) A semiconductor device, comprising:

a structure comprising at least two overlying layers of ~~epitaxially grown~~ epitaxial silicon, each epitaxial silicon layer ~~having~~ comprising a top surface~~,~~ and sidewalls ~~with an overlying layer of an~~, and insulative material~~,~~ over the sidewalls; an uppermost epitaxial ~~layer~~ silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; and the structure disposed on a substrate in a vertical orientation.

187. ~~(new)~~ The semiconductor device of Claim 186, comprising a transistor.

188. ~~(new)~~ The semiconductor device of Claim 187, wherein the structure comprises a transistor gate.

189. ~~(new)~~ The semiconductor device of Claim 187, wherein the structure comprises a source/drain diffusion region.

190. (amended) A semiconductor device, comprising:

a structure comprising at least two overlying layers of ~~epitaxially grown~~ epitaxial silicon, each epitaxial silicon layer ~~having~~ comprising a top surface and sidewalls, with ~~an overlying layer of an~~ insulative material over the sidewalls; an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; one or more of the at least two epitaxial silicon layers comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

191. The semiconductor device of Claim 190, comprising a transistor.

192. The semiconductor device of Claim 191, wherein the structure comprises a transistor gate.

193. The semiconductor device of Claim 191, wherein the structure comprises a source/drain diffusion region.

194. (new) A transistor in a semiconductor device, comprising:

source/drain diffusion regions disposed on a semiconductive region of a substrate; and

a transistor gate disposed on the semiconductive region between the source/drain diffusion regions, the transistor gate comprising two or more overlying layers of epitaxial silicon extending in a vertical orientation from the substrate, each epitaxial silicon layer comprising a top surface and insulated sidewalls; wherein a first epitaxial silicon layer is

disposed on the substrate, and a second epitaxial silicon layer is disposed on the top surface of the first epitaxial silicon layer; and an uppermost epitaxial silicon layer of the transistor gate comprises an insulated top surface.

195. (new) A transistor in a semiconductor device, comprising:

a transistor gate disposed on a semiconductive region of a substrate; and

an elevated source/drain diffusion region disposed on the substrate adjacent to the transistor gate in a vertical orientation from the substrate; the source/drain diffusion region comprising at least two overlying layers of epitaxial silicon including an uppermost epitaxial layer; each of the at least two epitaxial silicon layers comprising a top surface, sidewalls, and insulative spacers over the sidewalls; and the uppermost epitaxial layer having a top surface with an overlying layer of an insulative material.

196. (new) A semiconductor structure, comprising:

~~a structure comprising~~

at least two overlying layers of ~~epitaxially grown~~ epitaxial silicon, each of the at least two epitaxial ~~layer~~ silicon layers having a top surface, ~~and sidewalls with an overlying layer of an insulative material~~ sidewalls, and insulative spacers over the sidewalls; an uppermost epitaxial layer having a top surface with an overlying layer of an insulative material; one or more of the at least two epitaxial silicon layers comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

197. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface, sidewalls, and insulative material along the sidewalls; an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; and the structure disposed on a substrate in a vertical orientation.

198. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface, and insulated sidewalls; an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; one or more of the epitaxial silicon layers comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

199. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer having a top surface, sidewalls, and insulative spacers over the sidewalls; an uppermost epitaxial silicon layer having a top surface with an overlying layer of an insulative material; the structure disposed on a substrate in a vertical orientation; the structure being a component of a transistor.

200. (new) A semiconductor structure, comprising:

at least two overlying layers of epitaxial silicon, each epitaxial silicon layer having a top surface, sidewalls, and insulative spacers over the sidewalls; an uppermost epitaxial silicon layer having a top surface with an overlying layer of an insulative material; one or more of the at least two overlying layers of epitaxial silicon comprising a conductivity enhancing dopant; the structure disposed on a substrate in a vertical orientation; and the structure being a component of a transistor.

201. (new) A semiconductor device, comprising:

a structure comprising at least two overlying layers of epitaxial silicon, each epitaxial silicon layer having a top surface and insulated sidewalls; an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; and the structure disposed on a substrate in a vertical orientation.

202. (new) A semiconductor device, comprising:

a structure comprising at least two overlying layers of epitaxial silicon, each epitaxial silicon layer comprising a top surface, and sidewalls covered by an insulative material; an uppermost epitaxial silicon layer of the at least two overlying epitaxial silicon layers having a top surface with an overlying layer of an insulative material; one or more of the epitaxial silicon layers comprising a conductivity enhancing dopant; and the structure disposed on a substrate in a vertical orientation.

203. (new) A semiconductor structure disposed on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on the substrate; the first epitaxial silicon layer comprising sidewalls and a top surface;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first epitaxial silicon layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial silicon layer, the second epitaxial silicon layer comprising sidewalls and a top surface; and

depositing an insulative material layer thereover.

204. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer;

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; wherein, upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

205. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, depositing an insulative film over the underlying epitaxial layers, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

206. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, depositing an oxide film and removing a portion of the oxide film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, depositing an oxide film layer thereover, with no subsequent removal of the oxide film layer from the top surface of said uppermost epitaxial silicon layer.

207. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, depositing a nitride film and removing a portion of the nitride film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, depositing a nitride film layer thereover, with no subsequent removal of the nitride film layer from the top surface of said uppermost epitaxial silicon layer.

208. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate to about 450°C to about 950°C., and flowing at least one silicon precursor gas over the substrate at a rate of about 10 sccm to about 500 sccm, for about 15 seconds to about 30 seconds;

wherein, prior to selectively growing each epitaxial silicon layer, depositing an insulative film over the underlying epitaxial layers, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

209. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial layer at about 20 nm/minute to about 40 nm/minute;

wherein, prior to selectively growing each epitaxial silicon layer, depositing an insulative film over the underlying epitaxial layers, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

210. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial layer of less than about 10 nm/minute;

wherein, prior to selectively growing each epitaxial silicon layer, depositing an insulative film over the underlying epitaxial layers, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and

upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

211. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal oxidation, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal oxidation, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

212. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal nitridation, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal nitridation, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

213. (new) A semiconductor structure disposed on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on the substrate; the first epitaxial silicon layer comprising sidewalls and a top surface;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first epitaxial silicon layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial silicon layer while depositing a conductivity enhancing dopant, the second epitaxial silicon layer comprising sidewalls and a top surface; and

depositing an insulative material layer thereover.

214. (new) A semiconductor structure disposed on a substrate, the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on the substrate; the first epitaxial silicon layer comprising sidewalls and a top surface;

depositing an insulative layer thereover;

removing a portion of the insulative layer to expose the top surface of the first epitaxial silicon layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial silicon layer, the second epitaxial silicon layer comprising sidewalls and a top surface;

doping the second epitaxial layer with a conductivity enhancing dopant by ion implantation, and

depositing an insulative material layer thereover.

215. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure by heating the substrate and flowing at least one silicon precursor gas over the substrate at a rate and pressure to provide a growth rate of the epitaxial layer at about 20 nm/minute to about 40 nm/minute, wherein selectively growing at least the uppermost epitaxial layer comprises flowing the at least one silicon precursor gas with a conductivity enhancing dopant over the substrate; and

prior to selectively growing each epitaxial silicon layer, depositing an insulative film over the underlying epitaxial layers, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and,

upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

216. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface;

the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial layer, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial layer;

wherein, upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

217. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial layer, depositing a conductivity enhancing dopant at a variable rate to provide a concentration gradient of the dopant within the uppermost epitaxial layer;

wherein, upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

218. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial layer, depositing a

conductivity enhancing dopant at an increasing rate over time to provide a low to high concentration of the dopant within the uppermost epitaxial layer;

wherein, upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

219. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; wherein the uppermost epitaxial layer is selectively grown while doping, and upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

220. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure;

wherein, upon selectively growing the uppermost epitaxial silicon layer, doping the uppermost epitaxial layer with a conductivity enhancing dopant by ion implantation, and depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

221. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal oxidation, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and, during the step of selectively growing the uppermost epitaxial layer, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial layer; and

upon selectively growing the uppermost epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal oxidation, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

222. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface; the structure formed by a process comprising the steps of:

selectively growing overlying layers of epitaxial silicon to form a stacked, vertically oriented structure;

wherein, prior to selectively growing each epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal nitridation, removing a portion of the insulative film to expose the top surface of the preceding epitaxial layer, and selectively growing the epitaxial silicon layer on the exposed top surface of the preceding epitaxial layer; and, during the step of selectively growing the uppermost epitaxial layer, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial layer; and

upon selectively growing the uppermost epitaxial silicon layer, forming an insulative film over the epitaxial layers by rapid thermal nitridation, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.

223. (new) A stacked, vertically oriented semiconductor structure disposed on a substrate, the structure comprising overlying layers of epitaxial silicon including an uppermost epitaxial silicon layer; each epitaxial silicon layer having a top surface and sidewalls, and insulative material disposed on the sidewalls, and the uppermost epitaxial silicon layer comprises an insulative film disposed on the top surface;

the structure formed by a process comprising the steps of:

selectively growing a first epitaxial silicon layer on a substrate;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the first epitaxial layer;

selectively growing a second epitaxial silicon layer on the exposed top surface of the first epitaxial layer;

depositing an insulative film layer thereover;

removing a portion of the insulative film layer to expose the top surface of the second epitaxial layer; and

repeating the steps of selectively growing an epitaxial silicon layer, depositing an insulative film layer, and removing a portion of the insulative film layer to form the stacked structure; and during the step of selectively growing the uppermost epitaxial layer, depositing a conductivity enhancing dopant to form a concentration of the dopant within the uppermost epitaxial layer;

wherein, upon selectively growing the uppermost epitaxial silicon layer, depositing an insulative film layer thereover, with no subsequent removal of the insulative film layer from the top surface of said uppermost epitaxial silicon layer.